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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/812,267 | 03/29/2004 | Shaun Kazuo Wakumoto | 200400252-1 | 2764 |
| 22879 7590 07/25/2007 HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400 | | | EXAMINER JONES, PRENELL P | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/812,267

Applicant(s)

WAKUMOTO ET AL.

Examiner

Prenell P. Jones

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 July 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 9, 12 and 15-18 is/are rejected.
- 7) ☒ Claim(s) 7, 8, 10, 11, 13, 14, 19 and 20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 3/29/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 3-5, 9, 10, 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisco (Non-patent literature) in view of Moll et al (US PG PUB 20050078601) and Narvaez (US PG PUB 2004/0258062).

4. Regarding claim 1, Cisco discloses a switching environment wherein the architecture includes a plurality of Ipv6, Ipv4, 6PE routers communicating packets, wherein a hierarchy of labels are associated with routers, as well as router-ID (router identifier) and tag switching wherein resources (packets/paths) are tagged (Fig. 1-3 & 9, page 1, 5 and 19), whereby the routers are associated with a full mesh structure, Inserts tag into path (page 17, lines 19-25),

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and MAC rewrite and new MAC headers associated with CEFv6/Ipv6 routing table, which supports load balancing (page 15). Cisco further discloses hashing based on Ipv6 source/destination address, which is performed for load balancing (page 13), router/switch ID associated with MAC destination address/next address (page 18, 19, 26 and 27). Although, Cisco acknowledges table entries, hashing, tagging and index, he is silent on finding an entry in a switch table with a switch identifier, associating hash values with generating index values, tag tables associated with index value and inserting the path tag into the packet.

In a routing/switching environment wherein hash and route circuits are utilized, Moll discloses a packet routing scheme wherein the architecture includes switching devices, programmable hash for utilization of load balancing, wherein predetermined rules and paths are applied to predetermined fields in received packets to generate an index, which is used as a routing decision or access a routing table (Abstract, paragraph 0012, 0094), utilization of hashing to generate hashed values that are used to index into a routing table for outputting routing results, hash function is used as an index to a route table (paragraph 0014, 0015), hash values generated are utilized to index into route, and hash value are used to generate indexes which are base address tables (using hash value and associated data to generate an index value) (paragraph 0121, 0122), OVC/IQ output gives an index of the OVC, and a tag is interpreted as a IVC and OVC, and wherein an IVC is used to form an index into route tables, and wherein a route table index selects a route index from a data field of a path table (paragraph 0083, 0093, 0098, 0119), and a IVC/tag is carried in the packet (inserting a path tag into a packet) (paragraph 0046, 0047, 0078, 0103). In addition, Moll further suggests that the architecture include mesh topology (paragraph 0025), and switches that are associated with MAC addresses wherein the MAC addresses are associated with an address table/route table

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wherein the table includes destination addresses (Fig. 3 & 5, paragraph 0024, 0025, 0027, 0033, 0035, 0039, 0041 and 0045).

Furthermore, in another routing/switching environment wherein hashing and tagging are utilized, Narvaez discloses a switching system wherein packets are communicated, and the architecture includes load balancing, and system characteristics are stored in databases, such as forwarding information indicating source/destination with respect to transmission/routing of data, identifying MAC SA tag and DA tag for each router associated with the database, generated tags stored in memory/tag table/tag memory (Abstract, 0026, 0027, 0028, 0030), wherein hash value is used to index table interfacing nodes, utilizing tag lookup, priority tag lookup, MAC DA lookup (0015, 0064, 0066), and the index is associated with the new balance flow ID, which is obtained during a tag lookup (Fig. 2 & 6, paragraph 0064).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement finding an entry in a switch table with a switch identifier, associating hash values with generating index values, tag tables associated with index value and inserting the path tag into the packet as taught by the combined teachings of Moll and Narvaez with the teachings of Cisco for the purpose of further manage and increase routing efficiency.

Regarding claim 3, Cisco further discloses Ipv6 unicast-routing with respect to MAC destination/next and source address found in the MPLS table/MAC table (page 11, 14 & 16).

Regarding claim 4, Cisco further discloses hash function depending on MAC source and destination address (Fig. 3, page 9, 13, 16 & 17).

Regarding claim 5, further discloses hash function depending on IP source and destination address (Fig. 3, page 9, 13 & 17

Regarding claim 10, Cisco utilizes round-robin technique, which is weighted (pages 13 and 16).

Regarding claim 12, as indicated above, combined Cisco, Moll and Narvaez discloses a routing/switching environment that implements load balancing with the use of hashing, indexing and tagging resources wherein the architecture includes a plurality of Ipv6, Ipv4, 6PE routers communicating packets, router-ID, mesh structure, hashing based on Ipv6 source/destination address, router/switch ID associated with MAC destination address/next address, finding an entry in a switch table with a switch identifier, associating hash values with generating index values, tag memory/tables associated with index value and inserting the path tag into the packet, utilization of hashing to generate hashed values that are used to index into a routing table for outputting routing results, hash function is used as an index to a route table, and switches that are associated with MAC addresses wherein the MAC addresses are associated with an address table/route table wherein the table includes destination addresses and incoming packet is checked against entries in table.

Although Cisco and Moll fail to teach or suggest priority associated with the MAC addresses and the switch/device identifier, Narvaez further discloses devices and nodes can be identified according to flows, and once tag has completed processing, the tag will contain various characteristics, such as MAC DA, MAC SA, Priority ID, Priority tag, balanced flow ID, information to identify user/node (paragraph 0030, 0045, 0047, 0054, 0059, 0062, 0065, 0066, 0069).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement priority associated with the MAC addresses and the switch/device identifier as taught by Narvaez with the combined teachings of Cisco and Moll for the purpose of further implementing and managing load balancing within a switching environment.

Regarding claims 9 and 15, as indicated above, combined Cisco, Moll and Narvaez discloses a routing/switching environment that implements load balancing with the use of hashing, indexing and tagging resources wherein the architecture includes a plurality of Ipv6, Ipv4, 6PE routers communicating packets, router-ID, mesh structure, hashing based on Ipv6 source/destination address, router/switch ID associated with MAC destination address/next address, finding an entry in a switch table with a switch identifier, associating hash values with generating index values, tag memory/tables associated with index value and inserting the path tag into the packet, utilization of hashing to generate hashed values that are used to index into a routing table for outputting routing results, hash function is used as an index to a route table, and switches that are associated with MAC addresses wherein the MAC addresses are associated with an address table/route table wherein the table includes destination addresses and incoming packet is checked against entries in table.

Although Cisco and Moll fail to teach or suggest obtaining port number associated with index value in the tag tables/tag memory, Narvaez further discloses pre-configured values for ports/port number, and logical ports are configured to extract a type of tag, wherein load balancing of a single port over multiple ports is utilized, and the flow ID stored in the tag are utilized in the transmission of data (paragraph 0043, 0054, 0057).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement obtaining port number associated with index value in the tag tables/tag memory as taught by Narvaez with the combined teachings of Cisco and Moll for the purpose of further implementing and managing load balancing within a switching environment.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cisco (Non-patent literature) in view of Moll et al (US PGPUB 20050078601) and Narvaez (US PGPUB 2004/0258062) as applied to claim 1 above, and further in view of Higasiyama (US PGPUB 20040190454.)

Regarding claim 2, as mentioned above, combined Cisco, Moll and Narvaez discloses a routing/switching environment that implements load balancing with the use of hashing, indexing and tagging resources wherein the architecture includes a plurality of Ipv6, Ipv4, 6PE routers communicating packets, router-ID, mesh structure, hashing based on Ipv6 source/destination address, router/switch ID associated with MAC destination address/next address, finding an entry in a switch table with a switch identifier, associating hash values with generating index values, tag memory/tables associated with index value and inserting the path tag into the packet, utilization of hashing to generate hashed values that are used to index into a routing table for outputting routing results, hash function is used as an index to a route table, and switches that are associated with MAC addresses wherein the MAC addresses are associated with an address table/route table wherein the table includes destination addresses and incoming packet is checked against entries in table.

However, Cisco, Moll and Narvaez fail to teach or suggest receiving packets on a non-mesh port of a mesh switch. In a switching environment, Higasiyama discloses mesh network bridging wherein packets reach non-mesh connecting port (paragraph 0138, 0158, 0247, 0250, 0315, 0361). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement suggest receiving packets on a non-mesh port of a mesh switch as taught by, Higasiyama with the combined teachings of Cisco, Moll and Narvaez for the purpose of further implementing and managing load balancing within a switching environment, as well as minimizing contention.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cisco (Non-patent literature) in view of Moll et al (US PG PUB 20050078601) and Narvaez (US PG PUB 2004/0258062) as applied to claim 1 above, and further in view of Luke et al (US PG PUB 20040133634).

Regarding claim 6, as mentioned above, combined Cisco, Moll and Narvaez discloses a routing/switching environment that implements load balancing with the use of hashing, indexing and tagging resources wherein the architecture includes a plurality of Ipv6, Ipv4, 6PE routers communicating packets, router-ID, mesh structure, hashing based on Ipv6 source/destination address, router/switch ID associated with MAC destination address/next address, finding an entry in a switch table with a switch identifier, associating hash values with generating index values, tag memory/tables associated with index value and inserting the path tag into the packet, utilization of hashing to generate hashed values that are used to index into a routing table for outputting routing results, hash function is used as an index to a route table, and switches that are associated with MAC addresses wherein the MAC addresses are associated

with an address table/route table wherein the table includes destination addresses and incoming packet is checked against entries in table.

However, Cisco, Moll and Narvaez fail to teach or suggest hash function depending on TCP/UDP port numbers.

In a switching environment, Luke discloses load balancing wherein hashing is utilized in aiding in load balancing, whereby the architecture includes hash table index values are based on source/destination IP addresses and TCP/UDP port numbers (paragraph 0537).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement hash function depending on TCP/UDP port numbers as taught by Luke with the combined teachings of Cisco, Moll and Narvaez for the purpose of further implementing and managing load balancing within a switching environment.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 16 is rejected under 35 U.S.C. 102(e) as being anticipated by Moll et al (US PG PUB 20050078601).

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Regarding claim 16, Moll discloses a switching apparatus that implements load balancing, wherein the apparatus includes a memory controller 340 coupled indirectly to the plurality of switch ports of switch 310, and tagging associated with resources, such as virtual channels/IVC (Fig. 3, paragraph 0006, 0007, 0013, 0023, 0027, 0030, 0036, 0045, 0054, 0083, 0084, 0089, 0093, 0115).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moll et al (US PG PUB 20050078601) in view of Narvaez (US PG PUB 2004/0258062).

Regarding claim 17 and 18, as indicated above, Moll discloses a switching apparatus that implements load balancing, wherein the apparatus includes a memory controller 340 coupled indirectly to the plurality of switch ports of switch 310, and tagging associated with resources, such as virtual channels/IVC (Fig. 3, paragraph 0006, 0007, 0013, 0023, 0027, 0030, 0036, 0045, 0054, 0083, 0084, 0089, 0093, 0115). However, Moll is silent on Layer 2 Mac address table and tag table.

In a switching environment that utilizes load balancing in a system whereby software programs are utilized to implement function (paragraph 0055), Narvaez discloses Layer 2 MAC address table, wherein logical/physical ports or channels are monitored as resources, and logic is controlled by a selector mechanism/switch control device, and associating hash values with generating index values, tag memory/tables associated with index value and inserting the path tag into the packet, utilization of hashing to generate hashed values that are used to index into a routing table for outputting routing results, hash function is used as an index to a route table (Abstract, Fig. 2 & 6, 0015, 0064, 0066, 0064).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement Layer 2 Mac address table and tag table as taught by Narvaez with the teachings of Moll for the purpose of further implementing and managing load balancing within a switching environment.

Allowable Subject Matter

12. Claims 7, 8, 11, 13, 14, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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13. The following is a statement of reasons for the indication of allowable subject matter:

The combined prior art discloses a routing/switching mesh environment that implements load balancing with the use of hashing, indexing and tagging resources wherein the architecture includes a plurality of Ipv6, Ipv4, 6PE routers communicating packets, router-ID, mesh structure, hashing based on Ipv6 source/destination address, router/switch ID associated with MAC destination address/next address, finding an entry in a switch table with a switch identifier, associating hash values with generating index values, tag memory/tables associated with index value and inserting the path tag into the packet, utilization of hashing to generate hashed values that are used to index into a routing table for outputting routing results, hash function is used as an index to a route table, and switches that are associated with MAC addresses wherein the MAC addresses are associated with an address table/route table wherein the table includes destination addresses and incoming packet is checked against entries in table.

However, the combined prior art fails to teach or suggest with respect to claim 7 and 13, start index and total number of tags associated with switch identifier, with respect to claim 11, weighing includes a variable number of a same path tag in the tag table, wherein greater number of the same path tag corresponds to a greater weight for that tag, and with respect to claim 19, both a start index and a total number of tags associated with the switch identifier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Wing Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones

July 23, 2007


WING CHAN 7/23/07
SUPERVISORY PATENT EXAMINER